16.6 A 1.4V Signal Swing Hybrid CLS-Opamp/ZCBC Pipelined ADC Using a 300mV Output Swing Opamp

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Scaling in CMOS technologies has made the application of traditional opamp topologies increasingly difficult. In the face of decreasing voltage headroom and intrinsic device gain, designers have employed techniques such as gain-boosting, correlated double sampling , and correlated level-shifting (CLS) [1] to maximize output swing for a given gain specification. Zero-crossing based circuits (ZCBC) remove the opamp altogether and use a comparator and current sources [2], which are more amenable to scaling and have proven capable of high efficiency, as in [3]. However, the open loop nature of ZCBC creates challenges for designs that must reliably track over process, voltage, and temperature. In this paper, we describe a hybrid CLS-opamp/ZCBC pipelined ADC that introduces techniques to improve accuracy, robustness, and power efficiency in scaled technologies. It incorporates CLS and a low power, small output swing double-cascoded telescopic opamp to achieve very high effective gain. A dynamically biased zero-crossing detector (ZCD) is introduced that increases the power efficiency of ZCBC designs.

The basic operation of a CLS pipeline stage is shown in Fig. 16.6.1. The effective opamp gain at the end of Φ_2 is $A_{\Phi 1}A_{\Phi 2}$. A useful observation is that $A_{\Phi 1}$ and $A_{\Phi 2}$ do not need to be the same, or even come from the same opamp to benefit from CLS. Efficiency in the use of the CLS technique can be maximized by splitting the single opamp into two separate charging devices, each optimized for its unique set of requirements. In Φ_1, the opamp is connected directly to the output, and performs the majority of the charge transfer. During this time, high output swing and slew rate is desired. By contrast, in Φ_2 the opamp is coupled to the output via C_{CLS} and must slew and swing little; a high gain opamp in Φ_2 will help to maximize the structure's effective gain. The relaxed signal swing requirement allows high gain without the added power of gain-boosting amplifiers, and the low amount of slewing required means that power is only limited by linear settling requirements. For this design, a double-cascoded telescopic opamp was chosen.

For the Φ_1 coarse charging device, ZCBC topologies, which charge the output using current sources and detect the correct virtual ground condition with a ZCD, are well suited since the magnitude of the ZCD's current is constant and independent of the output charging currents. Furthermore, the ZCBC can be designed to dissipate zero current during the longer Φ_2 fine settling phase.

With no forced feedback, ensuring a robust ZCBC design across process, voltage, and temperature variations is problematic. Primary concerns are switch and current source linearity, and variation in ZCD time delay. By virtue of the opamp in Φ_2, the hybrid structure is able to exploit the power saving properties of ZCBC while alleviating all of these problems. The ZCBC must only be accurate enough to meet the output swing requirement of the opamp, which is determined by $A_{\Phi 1}$ and C_{CLS}.

The primary challenge of pairing a ZCD with an opamp is the differential output offset (or "overshoot") introduced by the ZCD's finite time delay between when its inputs cross to when the current sources turn off. When followed by opamp settling, as in this design, all components of the overshoot should be cancelled as best as possible. This can be done by controlling the ZCD input offset or by cancelling the overshoot at the output. For flexibility in testing, the latter was chosen.

As illustrated in the simplified schematic and timing diagram of Figs. 16.2.2 and 16.2.3, the hybrid MDAC amplification begins when the output nodes are pre-charged to V_{DD} and V_{SS}, the current sources (I_N, I_P) are turned on, shorting switches (S_{OP}) are enabled, and the cancellation DACs (C_{DAC}) are set to track the output. When the pre-charge switches (S_{PC}) open, the outputs begin charging until the ZCD triggers and I_N and I_P are turned off. The output of the ZCD then signals an asynchronous timing block, which flips the cancellation DAC sampling switches (S_{DAC}) to cancel the overshoot. After the DACs have settled, the asynchronous timing opens the shorting switches, allowing the opamp to begin settling until the end of the amplification phase.

To improve the power efficiency of the ZCBC, the dynamically biased differential ZCD of Fig. 16.6.4 is introduced. To minimize both the ZCD's absolute time-delay and variation in time-delay, a high g_m in the ZCD is needed when the inputs are close to crossing. Conversely, when the inputs are still far away (which is the case for most of the charging time), a higher g_m has little benefit. By concentrating the use of current around the detection instant, the g_m is maximized when most needed, and by proxy, the overall accuracy of the converter can be maximized for a given power budget.

The beginning of a zero crossing detection is started when switch M_3 opens and disconnects the tail source (M_1) from the DC bias. The tail current remains constant until $A_{ZCD}(V_{i+} - V_{i-}) \approx (V_{o+} - V_{o-})$. At that point, the voltage at V_{o-} will begin to rise, and via the feedback capacitor C_{FB}, V_b and I_{tail} will also rise. At the detection instant, the g_m of the ZCD is at a maximum. Once the ZCD decision is registered by the dynamic inverter at the output of V_{o+}, transistor M_2 shuts off the ZCD.

The speed of operation, the gain of the ZCD, and the size of C_{FB} all factor into how much the dynamic biasing will affect efficiency. Simulation results show that for the specifications of this design, the dynamic ZCD consumes at least 4 times less power than the ZCD of [3]. Furthermore, the higher g_m provided by the dynamic biasing makes this ZCD more immune to certain internal and external variations. In test, the ZCD bias current I_{ref} was varied between 6.5µA and 50µA with no change in performance. The overshoot cancellation DACs were set to the same code for all stages, indicating that the overshoot can be mitigated with a single global control.

Designed for testability and proof-of-concept, the prototype ADC consists of 10 identical 1.5b pipeline stages followed by a 1.5b flash backend. Application of common design techniques such as stage scaling, multi-bit, and opamp sharing, as well as the removal of the cancellation DACs in favor of a global ZCD input-offset control can be applied to significantly extend power efficiency.

Implemented in 0.18µm CMOS, the ADC achieves an ENOB of 11.1b with 20MHz clock. It consumes 14.9mW analog and 2.2mW digital power. SNDR is 68.2dB and SFDR is 76.5dB. The SFDR is limited by even harmonics, which were not present on a previous version of the test board, suggesting they may originate from outside the chip. The ADC maintains 66dB SNDR for f_{in} up to $f_s/2$. The FoM is 344fJ/conversion-step at 10MHz and 406fJ/conversion-step at 20MHz.

Acknowledgments:
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References:
[1] B.R. Gregoire, U. Moon, "An Over-60dB True Rail-to-Rail Performance Using Correlated Level Shifting and an Opamp With Only 30 dB Loop Gain," *ISSCC Dig. Tech Papers*, pp. 540-541, Feb. 2008.
[2] T. Sepke, J. K. Fiorenza, et al., "Comparator-Based Switched-Capacitor Circuits for Scaled CMOS Technologies," *ISSCC Dig. Tech Papers*, pp. 220-221, Feb. 2006.
[3] L. Brooks, H-S Lee, "A 12b 50MS/s Fully Differential Zero-Crossing Based ADC Without CMFB," *ISSCC Dig. Tech. Papers*, pp.166-167, Feb. 2009..

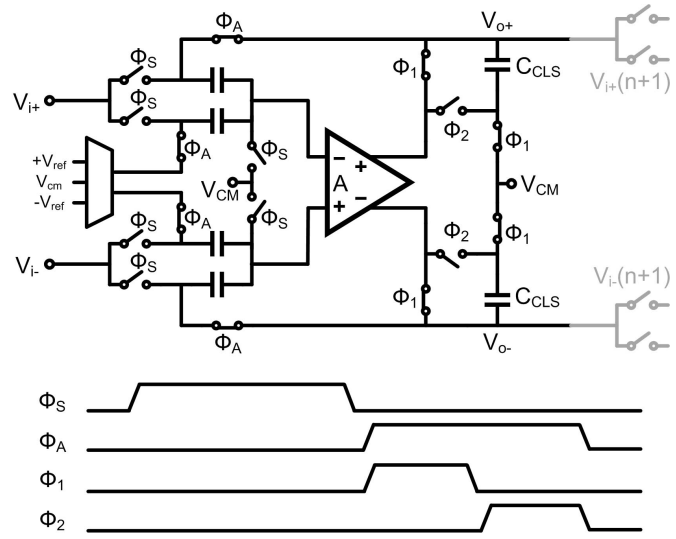

Figure 16.6.1: Correlated level-shifting (CLS) pipelined structure.

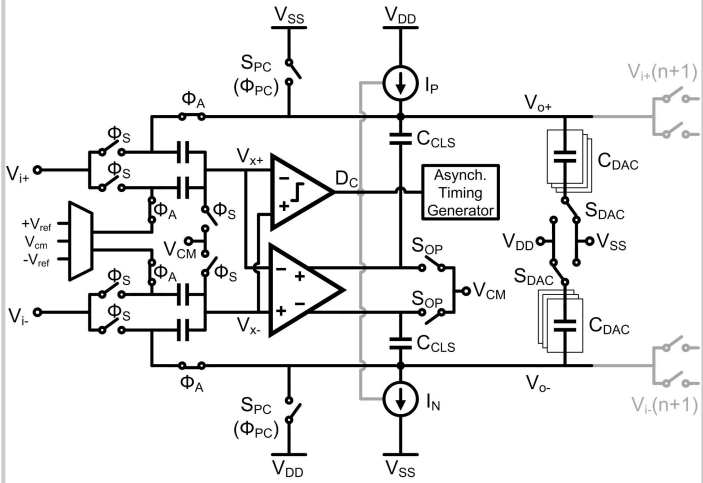

Figure 16.6.2: Simplified hybrid CLS-Opamp/ZCBC.

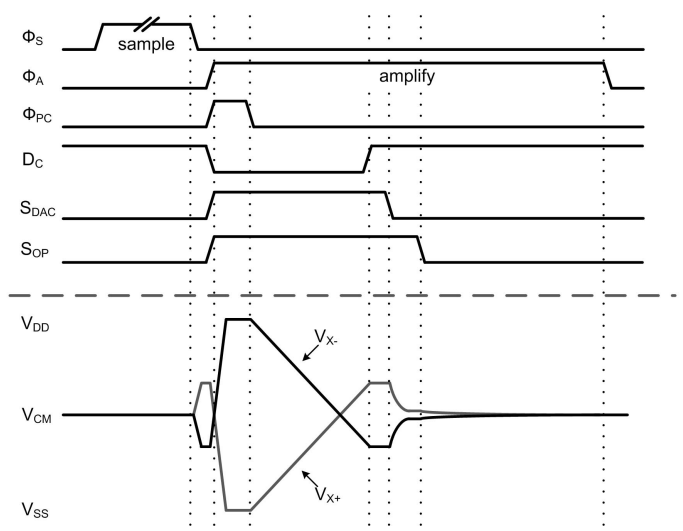

Figure 16.6.3: Simplified timing diagram for hybrid structure.

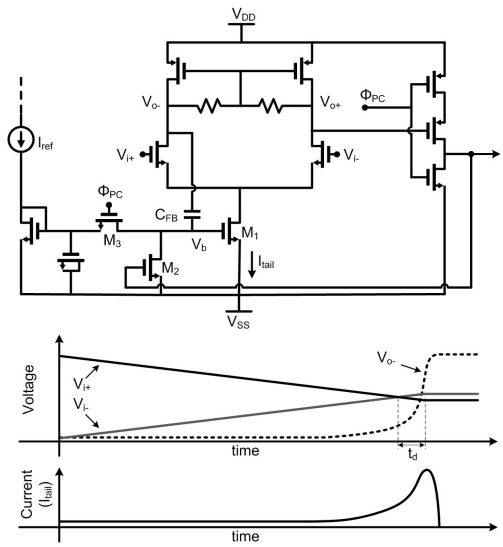

Figure 16.6.4: Simplified dynamicaly biased ZCD.

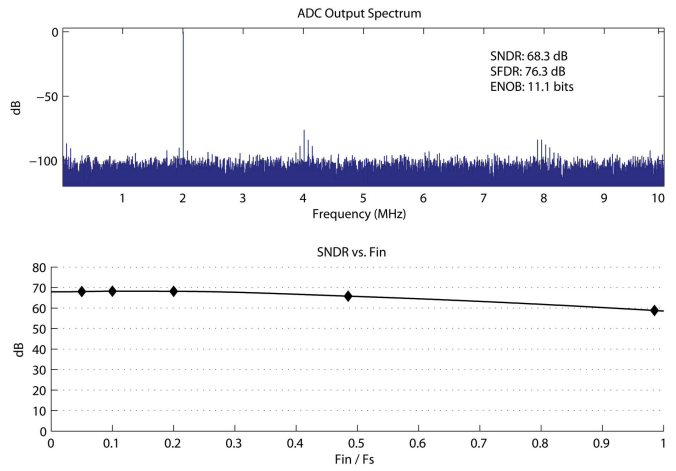

Figure 16.6.5: Measured output spectrum and plot of SNDR vs. fin from 0 to twice nyquist, both at 20MHz sampling.

Technology	0.18µm CMOS			
Supply Voltage	1.8V			
Input Voltage Range	1.4V			
Sampling Frequency	f_S = 10 MHz		f_S = 20 MHz	
ENOB	11.3b		11.1b	
SNR	69.6dB		68.3dB	
SNDR	69.5dB		68.3dB	
SFDR	78.8dB		76.3dB	
Power (analog/digital)	7.2mW	1.2mW	15.0mW	2.2mW
FoM	343.5 fJ/step		405.5 fJ/step	

Figure 16.6.6: Table of Measured Results.

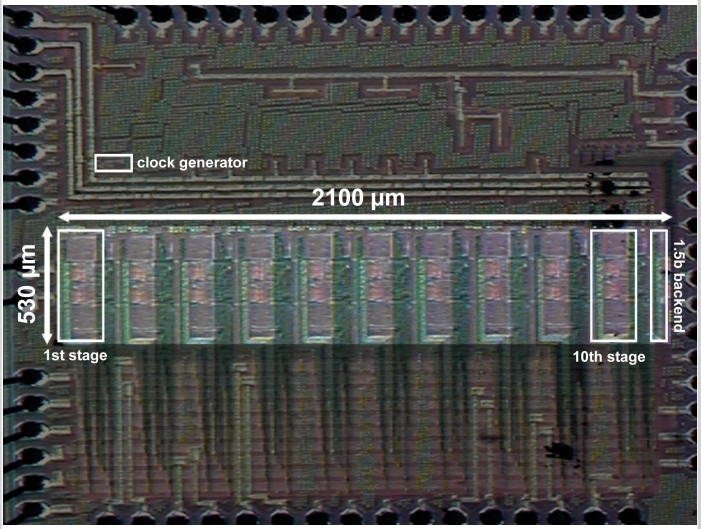

Figure 16.6.5: Micrograph, 0.18µm CMOS.

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